simulation of digital circuits,
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ON ENHANCING DIAGNOSTIC EFFECTIVENESS OF AUTONOMOUS TEST STRUCTURES FOR DIGITAL CIRCUITS OF MEDICAL DEVICES

The problem of reliability of medical electronic systems (EMD) controlled by a digital subsystem is discussed. The environmental security of EMD results from conformance to standards applying to design, manufacture, testing and implementation (in the USA, Department of Heath & Human Services, Food and Drug Administration and Quality System Regulation QSR [6]). These standards describe the whole life cycle of a device and apply both to hardware and software. However, it is impossible to eliminate completely all failures, faults and defects; some of them could have catastrophic effects to the environment. This is why digital circuit tests are of utmost importance to ensure reliability of digital systems, thus also proper diagnostics and care of the patient's health and life.

The researches on design of more effective digital circuit self-testing and minimizing them are of particular significance in such important applications as medical procedures that use EMD.

1. INTRODUCTION

The Electronic Medical Devices (EMD) such as cardio-monitoring, defibrillators, electrocardiographs, measuring server and other healthy systems, should provide dependability of rendered services in the terms of service availability and reliability, safety, environmental impact and protection against unauthorized use. Nowadays, the EMD, besides its specific analog parts are equipped with an appropriate controlling digital system. The digital system is responsible for data acquisition, processing, collecting, availability and transfer, and is achieved with boards of integrated circuits as well as appropriate software; quite often there are microprocessor systems. As regards to analog part, the security of EMD results from the required standards to be met to allow implementation in medical practice. These standards predict not only procedures for implementation but even servicing procedures [5]. The safe EMD excludes the occurrence of catastrophic failures to the environment, thus also to human health and life.

The diagnostics if microprocessor systems includes power on self-test (POST), in particular of CPU, interrupts and threads, EEPROM and its checksums, DRAM in the terms of proper writing and reading, DMA controllers and other peripheral devices and rendered services, also those of interfaces, loop back test as well transient and link error monitoring. The software testing, besides single tests, applies also to problems of deadlock, software incompatibility within the middleware layer or data buffer overflow, especially in embedded systems [7].

Currently, the programmable systems of FPGA type are commonly used. These systems allow implementation of combinational and sequential circuits as well as application specific circuits, e.g. encoders/decoders, communication systems, microprocessors. Nowadays, the FPGA circuits often replace even Medium Scale Integration (MSI) circuits due to its high programming capability. The FPGA circuits are also used in small lot production of application specific circuits of ASIC type. To achieve good operating parameters and to reduce manufacturing costs the complete digital systems in one integrated circuit – system-on-chip (SOC) - are often used. In SOC the virtual Intellectual Property modules (IP CORE) are employed to perform different modular functions. The SOCs eliminate the problem of distribution of many circuits on a printed circuit board (PCB) and facilitate keeping of operating parameters of such integrated circuits.

Failures, faults and defects break reliability of digital circuits. Failures arise mainly from imperfection of the manufacturing processes, and rarely result from improper use or design. Failures of integrated circuits are of various nature and one can distinguish stuck at 0 or stuck at 1, synchronization

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and delay failures, bridging faults, open faults, and in the case of MOS failures may consist in transistor stuck on or stuck off in a logical gate. Some faults have no logical representation. In the case of high timing frequency, faults related to connection impedance parameters may occur.

The stimulated fault may manifest itself as an error, and the detected error indicates a fault understood as a breach of the digital circuit functional specification. The useful information on fault in the form of error can be achieved due to its propagation into circuit output, thus requiring adequate propagation conditions for error signal. This is the domain of digital circuit testing.

There are known methods for keeping reliability of digital circuits, including fault prevention, fault tolerance, fault removal and fault forecasting, often redundant with the use of error detection and correction codes. The application of signal encoding reduces data susceptibility to noises and interferences, that often could not be eliminated completely. Some data redundancy in encoding is commonly used, for example, in data transmission and compression in general purpose applications.

Testing and self-testing can be assigned to reliability providing means, particularly for validation, understood in general as fault prevention and removal. The fault elimination in turn is related to verification, diagnostics and correction, while testing and self-testing of digital circuits provide verification and enable diagnostics [3].

Testing and self-testing of digital circuits are in principle the off-line diagnostics domain as regards to recognition of circuit operational abnormality. Such diagnostics is performed when the circuit is idle, thus faults should not be localized but only serviceability or unserviceability of the tested circuit must be decided. Embedding the whole or major part of the tester into the circuit is considered as Built-In-Self-Test (BIST), that can be implemented with the linear technique – independent Test Pattern Generator (TPG) and Test Response Compactor (TRC) (with Linear Feedback Shift Registers LFSR and Multi Input Signature Registers MISR), or by employing nonlinear technique with Self-Test Path (STP) or circular STP (CSTP). Some modifications of these self-testing techniques are also known. Contrary to linear technique, the tested digital circuit in nonlinear technique is a feedback of STP or CSTP, thus posing a problem with parameter selection for these structures. Nevertheless, simulations presented in this paper, show that it is possible to design such Autonomous Test Structures (ATS) that achieve higher effectiveness than those of solutions reported in the literature and often are minimized. The minimization consists in the concept of external self-testing, where internal memory module (MM) of the circuit is disconnected during test, thus no additional conditions are imposed on its operation. It should be noted that both in linear and nonlinear testing techniques, the circuit MM is typically included into self-testing structure registers, as results from ability to improve testability and application of Design for Testability (DFT).

In this paper an effect of implementation of MM subsets of the tested circuit on diagnostic effectiveness of ATS is also presented. The measure of effectiveness is Fault Coverage (FC). The structures discussed here pass over implementation requirements into FPGA systems, but as mentioned above, sequential circuits can be implemented into such systems by employing various techniques [4]. The enhancement of testing effectiveness is a task related to reliability of digital circuits, and its minimization results from limited number of FPGA system components that affect self-testing.

2. AUTONOMOUS TEST STRUCTURE

The block diagram of STP and CSTP structure for combinational system [1], valid also for a sequential system in external self-test as defined below is presented in Fig. 1.

Definition 1. External Self-Test.

External Self-Test to be understood as a self-test of a sequential system in which the memory block MM is not included into the register of STP or CSTP (is not disconnected during test).

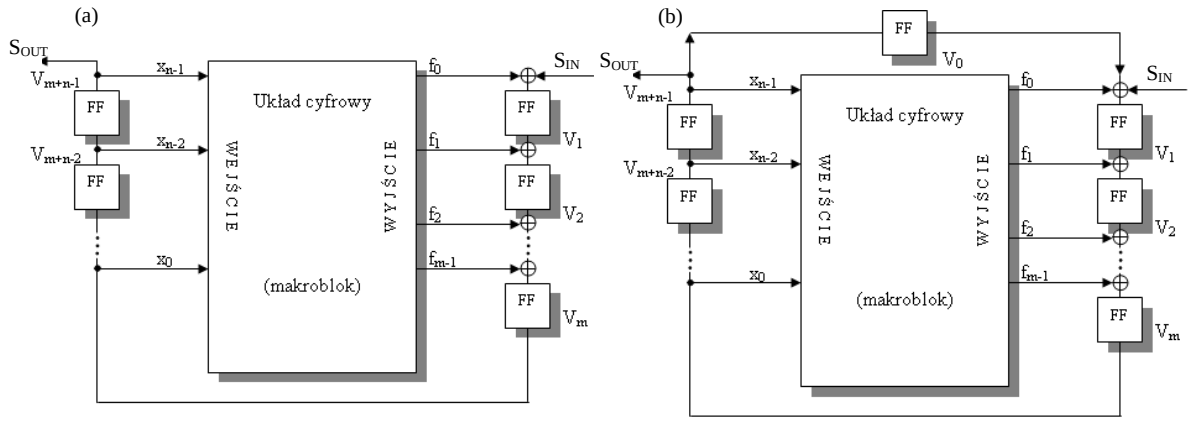

Fig. 1. Autonomous Test Structure (a) Self-Test Path, (b) Circular Self-Test Path.

The functioning of STP/CSTP structure can be described by equation (1).

$$[V(t+1)] = [T] \cdot [V(t)] \oplus [F(V(t))] \tag{1}$$

where:

$[V(t)]$ – state of the register at moment t,
$[V(t+1)]$ – state of the register at next moment t+1,
$[F(V(t))]$ – system response matrix,
T – connection matrix.

The model of ATS presented in Fig. 1 can be extended by additional components to allow linear feedback selection and also responsible for configuration of the STP or CSTP register connections with the tested sequential circuit [2]. The connection matrices distinguished with the suffix FREE enable even the XOR matrix structure to be created, while matrices denoted with the suffix LONG may lead de facto to condensed STP or CSTP registers.

By including matrix [OM], allowing configuration changes of output connections of the tested circuit with STP/CSTP register, into equation (1), we obtain (2):

$$[V(t+1)] = [T] \cdot [V(t)] \oplus [OM] \cdot [F(V(t))] \tag{2}$$

The product of matrices $[OM] \cdot [F(V(t))]$ can be expressed more precisely in the form (3).

$$\begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 1 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 1 & \cdots & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 & 0 & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & 0 & 0 & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \bullet \begin{bmatrix} 0 \\ f_0(V_m(t),...,V_{m+n-2}(t),V_{m+n-1}(t)) \oplus S_{IN}(t+1) \\ f_1(V_m(t),...,V_{m+n-2}(t),V_{m+n-1}(t)) \\ \vdots \\ f_{m-1}(V_m(t),...,V_{m+n-2}(t),V_{m+n-1}(t)) \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} \tag{3}$$

Depending on the contents of the minor (marked in grey in formula (3)) the three types of output connection matrices can be distinguished:

- OUTPUT MATRIX E, unit matrix that remains the nature of connections unchanged,
- OUTPUT MATRIX 1, a matrix that contains single 1 in each row and each column,

– OUTPUT MATRIX FREE, a matrix that may contain more than single 1 in each row and each column.

The same notation can be applied to input connection matrices of INPUT MATRIX type.

The following linear feedback types can be chosen when configuring the ATS model:

1. AIJ TOP-BOTTOM LFSR (1-1500), additional external and internal linear feedbacks are possible,
2. BOTTOM LFSR (1500-3000), additional internal linear feedback is possible,
3. SHIFT REGISTER (3000-4500), no additional linear feedback,
4. TOP LFSR (4500-6000), additional external linear feedback is possible,
5. TOP-BOTTOM LFSR (6000-7500), additional external and internal linear feedbacks (other than AIJ TOP-BOTTOM LFSR) are possible.

To configure the STP/CSTP register connections with the tested circuit, the following connection diagram types were distinguished:

1. for circuit inputs:

– INPUT MATRIX 1 (1-300), complex connections available to the part of the STP/CSTP register that controls inputs of the tested circuit,
– INPUT MATRIX 1 LONG (300-600), complex connection, while allowing connections with any component of the STP/CSTP register,
– INPUT MATRIX E (600-900), simple connections (as shown in Fig. 1),
– INPUT MATRIX FREE (900-1200), connections through XOR matrices, but only with those STP/CSTP register components that control inputs of the tested circuit,
– INPUT MATRIX FREE LONG (1200-1500), connection through XOR matrices with any STP/CSTP register components.

2. for circuit outputs:

– OUTPUT MATRIX 1 (1-100), complex connections, available for those components of STP/CSTP register that are responsible circuit response.
– OUTPUT MATRIX E (100-200), simple connections (as shown in Fig. 1),
– OUTPUT MATRIX FREE (200-300), connections through XOR matrices, but only with those STP/CSTP components that are responsible for circuit response receiving.

The matrix names listed above contain the type of linear feedback and connection matrix. In brackets there are identifiers being useful in analysis of simulation graphs presented in Figures 2 and 3. For example, the ATS identifier equals 5100 – indicates an ATS with additional linear feedback of TOP LFSR type and the input connection matrix INPUT MATRIX 1 LONG enabling connection of the tested circuit input with any STP or CSTP register component, and the output connection matrix OUTPUT MATRIX FREE, allowing an additional XOR matrix structure containing logic functors of the exclusive sum ExOR to be generated.

To determine a relationship between the specified ATS configuration and the sequence length generated by such structure as well as the gained value of FC, numerous simulations were made for various ATS examples. These relationships obtained for 75 different ATS configurations, each of 100 statistical tests with randomly chosen ATS initial parameters are presented in Fig. 2. This includes such parameters as the form of connection matrix, additional linear feedback and the initial state of the register.

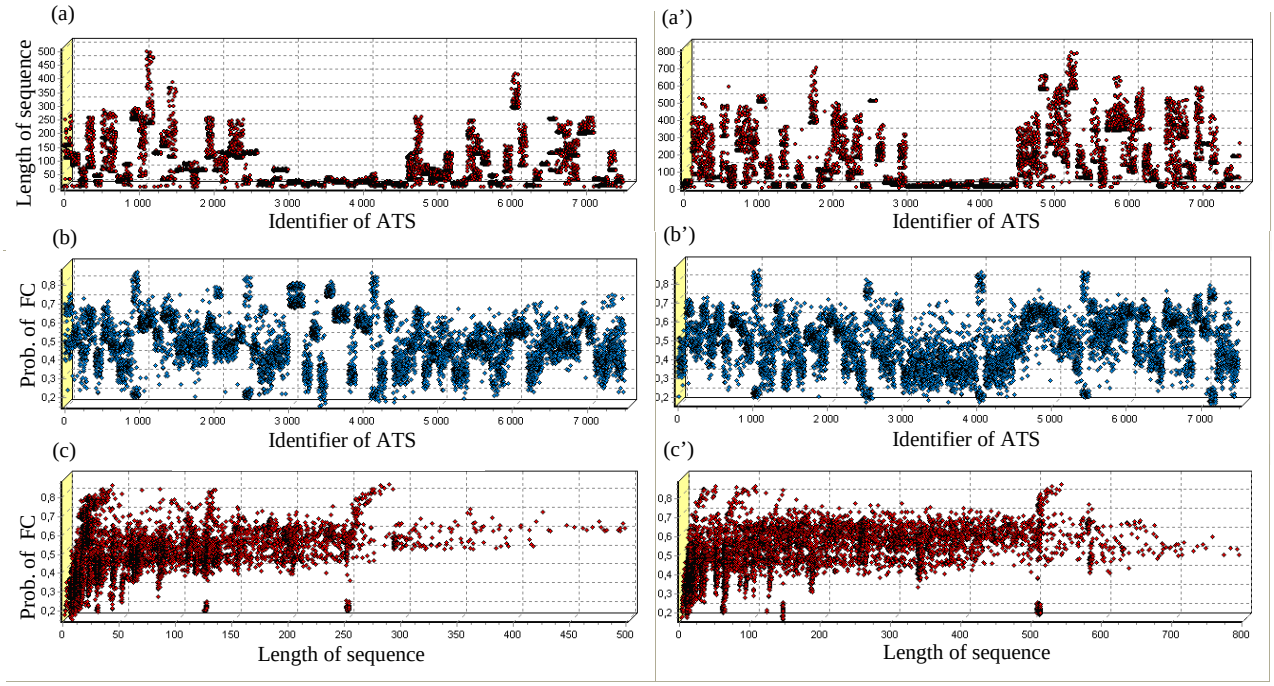

Fig. 2. 7500 different ATS for s298 without connecting MM components of the circuit (a) – Length of sequence vs. STP, (a') – CSTP, (b) – Probability of FC vs. STP, (b') – CSTP (c) – Overall probability of FC vs. length of sequence for 7500 different ATS – STP, (c') – CSTP.

It follows from Fig. 2, that although the simple ATSs based on STP and CSTP (Fig. 2.a and 2.a' Identifier of ATS: 3000-4500) generate relatively short sequences, they enable relatively high FC values to be obtained (Fig. 2.b, 2.b' Identifier of ATS: 3000-4500). Within the same area one may observe an increased correlation between the length of generated sequence and the FC value for STP compared to that of CSTP. Fig. 2c and 2c' presents an aggregated graph of the relationship between FC and the test sequence length.

Including 7 randomly chosen MM components of the tested circuit to ATS significantly increases the length of generated sequence and the value of FC. When comparing graphs presented in Fig. 3a and 3a' it should be noted that CSTP generates statistically larger number of longer sequences than STP, while the values of FC remain comparable (Fig. 3b and 3b'). It should be noted that the tested circuit s298 to which the graphs presented in Fig. 2 and 3 apply, has 14 MM components. For various ATS with included 7 MM components of this test circuit, the values of FC reach unity, as indicated in Table 1 in the row assigned to the circuit s298 (*FC=0.997). Such value of FC declassifies the solutions available in the literature referenced also in Table 1. There are also more concentrated cluster areas visible in Fig. 3b and 3b' which should be interpreted as a stronger correlative relationship between ATS and FC values, particularly the area shown in Fig. 3b', for ATS identified with 4900, indicates a low diagnostic effectiveness of such structure type (FC<0,5). The structure 4900, as described above, encodes CSTP with allowable additional ExOR logical gates of an external linear feedback by employing a configuration of INPUT MATRIX 1 LONG and OUTPUT MATRIX E; such configuration may take a condensed form due to influence of input connection matrix of this type, and in consequence – could reduce the length of CSTP register, thus also reduce the FC values.

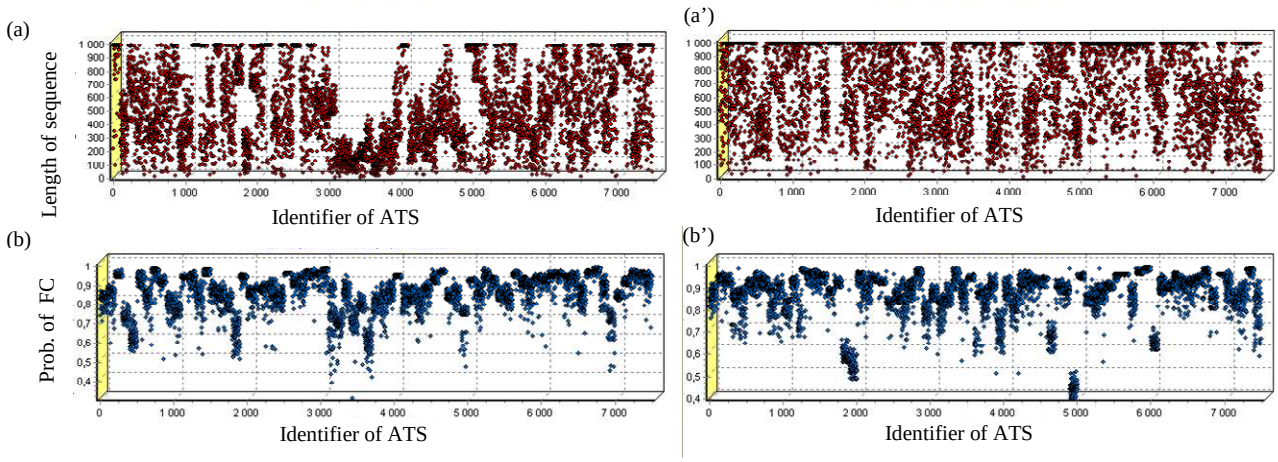

Fig. 3. 7500 different ATS (s298) with connected 7 MM components of the circuit (a) – Length of sequence vs. STP, (a') – CSTP, (b) – Probability of FC vs. STP, (b') – CSTP.

3. SET OF TEST CIRCUITS AND RESULTS

In Table 1 the FC values obtained for a subset of ISCAS'89 sequential test systems are presented by employing different design methods, often with the use of genetic algorithms (GATTO, GATTO+, GATTO*, SELFISH GENE GA) and deterministic systems based, among other things, on Automatic Test Pattern Generation (ATPG), Cellular Automata (CA) and Finite State Machines (FSM), and Binary Decision Diagrams (BDD) [8].

Table 1. Comparison of design methods and FC test structures.

Test Structure/ Used Algorithm	Test Circuits (subset of ISCAS'89 Benchmark)												
	S208.1	S298	S349	S382	S444	S641	S713	S820	S953	S1196	S1238	S1423	S1494
	Fault Coverage												
In this paper	0.995	**0.889** **0.997 ***	**0.991**	0.882	0.875	**0.921**	**0.862**	0.493	0.987	0.891	0.836	0.530	0.714
GATTO	0.679	0.886	NA	0.917	0.890	0.873	0.826	0.918	NA	0.995	0.946	0.963	0.847
CA2	0.673	0.876	0.973	0.877	0.863	0.873	0.826	0.598	0.983	0.832	0.812	0.882	0.877
ATPG	0.677	0.876	0.978	0.949	0.926	0.873	0.826	0.949	0.990	0.997	0.945	0.896	0.964
GATTO	0.679	0.886	NA	0.917	0.890	0.873	0.826	0.918	NA	0.992	0.946	0.963	0.847
ATPG-LP	1.000	0.877	0.984	0.927	0.924	0.874	0.877	0.529	0.991	0.995	0.960	0.973	0.972
GATTO+	0.697	0.886	0.978	0.947	0.924	0.873	0.826	0.941	0.991	0.995	0.944	0.967	0.960
CSTP	0.748	0.886	0.833	0.883	0.831	0.834	0.841	NA	NA	0.641	0.622	NA	NA
FSM-ATPG	0.976	0.913	0.954	0.286	0.317	0.887	0.848	0.965	0.995	0.999	0.971	0.445	0.984
CA-GA	1.000	0.893	0.959	0.943	0.924	0.886	0.846	0.528	0.993	0.894	0.954	0.445	0.960
HITEC	NA	0.860	0.954	0.754	0.787	NA	NA	0.956	NA	NA	NA	0.518	NA

HITEC-BDD	NA	0.860	0.957	0.779	0.820	NA	NA	0.956	NA	NA	NA	0.564	NA
CCPS	1.000	0.893	0.968	0.943	0.924	0.886	0.846	0.528	0.993	0.894	0.854	0.866	0.960
CA 90/150	0.948	0.238	0.610	0.165	0.138	0.886	0.847	0.456	0.994	0.942	0.915	0.635	0.559
SELFISH GENE GA	1.000	0.895	0.806	0.942	0.923	0.887	0.847	0.479	0.994	0.953	0.919	0.876	0.929

The external self-test technique despite of its lower testability, has reached evidently higher advantage over less complicated test circuits (s208.1, s298, s349, s641, s713). For some test circuits of medium degree of complexity (s382, s444, s953) the obtained FC values are comparable to those of other test design methods or test pattern generating structures. The largest disadvantageous differences for external self–testing are visible in simulations of circuits s1196, s1238 and s1494. Some test circuits (s820, s1423) are so specific that rather deterministic test techniques (ATPG) than pseudorandom tests shall be used. It should be emphasized the test length parameter was reduced to 1000 test vectors, and while such length seems to be sufficient for less complicated circuits, it is significantly too low for circuits of medium degree of complexity (typically the length of test for such circuits is counted in tenths thousands of test excitation vectors). Surely such limitation of test length led to increased advantage of FC valuation for other structures compared to external self-test technique presented in this paper. However, this limitation is justified by examination up to 75 different ATS types, each with 100 statistical tests with randomly chosen parameters affecting diagnostic effectiveness of STP and CSTP.

4. CONCLUSIONS

An effect of implementation of some MM subsets into ATS on increasing testability of sequential digital circuits is demonstrated. The positive results of experiments indicate that external self-tests of sequential circuits are possible without any intervention in its operational specification; in consequence ATS may be significantly simpler, while no special requirements related to memory module design are imposed. However, ATS is not always sufficiently effective in external self-tests and then even a small subset of MM of the tested circuit should be included into its structure to improve significantly the obtained lengths of generated sequence and FC, as evidenced by simulations. It seems that it is possible to reduce significantly an effect of AO on built in autonomous test structure ATS and hierarchical tests of digital circuits, boards and systems of electronic medical devices.

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