

*programmable circuits
ECG acquisition with cardiostimulator pulse*

Leszek DREWNIOK^{*}, Janusz ZMUDZINSKI^{*},
Jerzy GALECKA^{*}, Adam GACEK^{*}

APPLICATION OF PROGRAMMABLE LOGIC DEVICES FOR ACQUISITION OF ECG SIGNAL WITH PACEMAKER PULSES

The paper describes implementation of a new technology of digital systems design in case of medical measurement interface of IMPULS system used for acquisition of ECG signal from pacemaker patients. Similarly as in other applications, the processor circuit is a base of digital system, however – regarding large number of performed tasks – it is assisted by additional peripheral logic circuits. At the beginning, there were used standard elements (logic gates, counters, registers, etc.), however a growing complexity of beyond processor operations encouraged designers to apply the programmable circuits. The paper presents the stages of digital system development that has been implemented in medical measurement interface. It is the excellent example of possibility to integrate several standard elements in one integrated circuit.

1. HISTORY OF PROGRAMMABLE CIRCUITS

Programmable circuits became an alternative for standard elements of medium and large integration scale. Generally, they can be divided into specific circuit type – Application of Specific Integrated Circuits (ASIC) as well as universal Programmable Logic Devices (PLD) circuits. The circuits of ASIC type are produced for definite applications and do not allow to change the interconnection configuration after being produced, whereas PLD circuits have universal logic blocks, configuration of which can be adapted to specific application. The network of interconnections can be programmed after production of integrated circuit, and in case of reprogrammable structure – even many times modified.

So to say, the first representative of PLD circuits was a ROM memory that was used only for data storage and not as a logic circuit. PLD circuits were introduced into production in later period. Regarding the organisation of logic elements and other features, these PLD circuits have been divided into the following circuit types: PAL (Programmable Array Logic), GAL (Generic Array Logic), MACH (Macro Array CMOS High-density), EPLD (Erasable PLD), PLS (Programmable Logic Sequencer) and FPGA (Field-Programmable Gate Array) including LCA (Logic Cell Array) [1] [2].

The first PAL circuit was made in 1977 by MMI Company [1]. Basic structure contained the programmable matrices AND and OR (Fig.1).

^{*} Institute of Medical Technology and Equipment, 41-800 Zabrze, Roosevelta 118

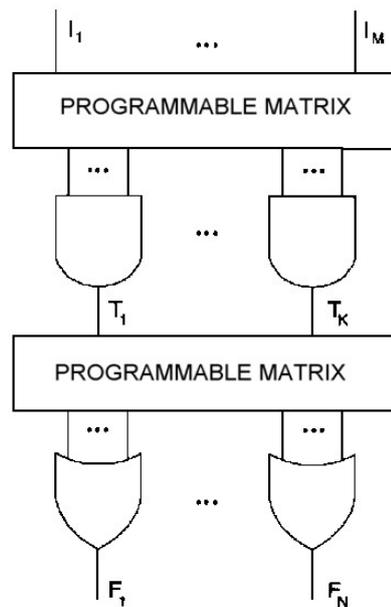


Fig.1. Basic PLD structure [1]

Basing on this structure, there were designed its various options containing one of the matrices without the programming possibility. There were also developed AND/OR structures connected with flip-flop and three-state gate enabling the application of given circuit output as an input or output for digital signals.

The structures with separate internal macrocells and I/O macrocells were the next stage of development. Fig. 2 presents the general structure based on this model.

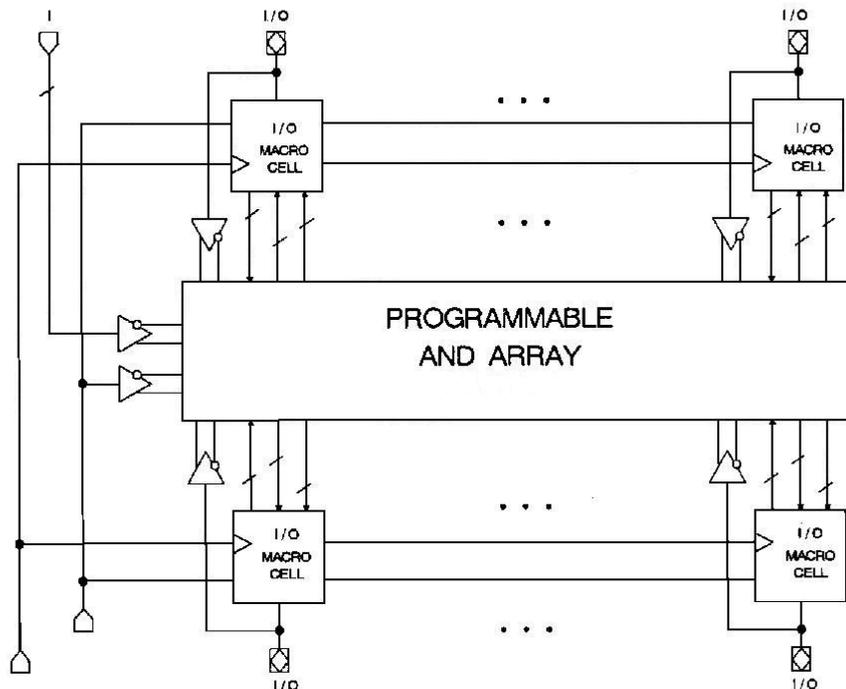


Fig.2. Structure with separate macrocells [1]

With time, the circuits were developed with a multi-matrix structure (eg. MACH circuits) containing many blocks of PAL type that communicated each other via so called Switch Matrix.

Nowadays the PLD circuits contain in their structure not only basic logic circuits but also memory blocks, specialised processor blocks and even analog blocks (such as A/D and D/A converters, amplifiers, comparators, filters etc.) [5]. There is a constant progress of integration degree so – for instance – for present technology of 0,13 μm one PLD circuit comprises over 100.000 logic elements, over 10 Mbits of RAM memory, up to 28 DSP blocks, over 200 blocks used for multiplication operations, over 10 phase loops as well as over 1300 universal I/O ports (circuits from a Stratix family of Altera company – EP1S120) [4].

2. ADVANTAGES OF DESIGNING WITH PLD STRUCTURES

Among the most important advantages of designing with the use of PLD structures are:

- possibility to change configuration without the necessity of printed circuit redesign,
- possibility of functional changes and addition of new modules in any stage of production,
- merging of many modules in one integrated circuit, which means the reduction of path number and the area occupied,
- possibility to select the tool of structure description – e.g. by means of a diagram, waveforms, Hardware Description Language (HDL),
- possibility to accurately simulate the physical action with the use of simulation modules integrated with design environment,
- possibility of actualisation of digital system already used by a client.

In the area of fixed heart stimulation, observed is the permanent search for more advantageous technical hardware solutions and new ways of pulses application ensuring the betterment of hemodynamic effects. When designing the measurement device for pacemakers, it is difficult to determine all the functions the device will have to perform in the future. Therefore, the application of configurable digital system based on PLD circuit is an optimum solution making possible its adaptation to permanently changing needs.

3. DEVELOPMENT STAGES OF MEDICAL MEASUREMENT INTERFACE

Medical measurement interface developed in our Institute is intended for acquisition of ECG signals from the surface leads containing pulse artefact from implanted cardiostimulator. The pulse form provides a lot of valuable information on stimulator-electrode-patient circuit and enables the detection of many abnormalities during a fixed stimulation. Because the width of pulses generated by a stimulator equals from tens microseconds to single milliseconds, in order to reflect the pulse form, the sampling frequency shall be considerably larger than sampling frequency of ECG signal (minimum 100 kHz per channel).

To avoid the employing of processor in current handling of fast converters, there has been designed the peripheral circuit aimed at recording of pulses from two ECG leads and then rendering accessible the whole sample package for analysis by the processor. During design process, the model peripheral circuit – consisted of FIFO memory and standard logic elements – has grown up

to several integrated circuits. The main reason of this was a necessity to store the samples before pulse detection to have a possibility to record correctly the pulse leading edge. The decision was taken to implement entire control circuit composed of counters, registers and gates into one PLD circuit. The EPF8282 circuit (having features presented in table 1) of Altera company has been selected.

Feature	Usable gates	Flipflops	Logic array blocks (LABs)	Logic elements (LEs)	Maximum user I/O pins
EPF8282	2500	282	26	208	78

Tab.1. Features of EPF8282 circuit

Initially, the programming of this circuit was effected with Active Parallel (AP) method, and the interconnection network was contained in a standard parallel EPROM memory. In the next stage, the AP method was replaced by Active Serial (AS) method and the configuration program was contained in serial memory of PROM type. In both cases, the interconnection configuration proceeded each time after supply was switched on. Fig. 3 presents a block diagram of first version of the stimulator pulse recording circuit.

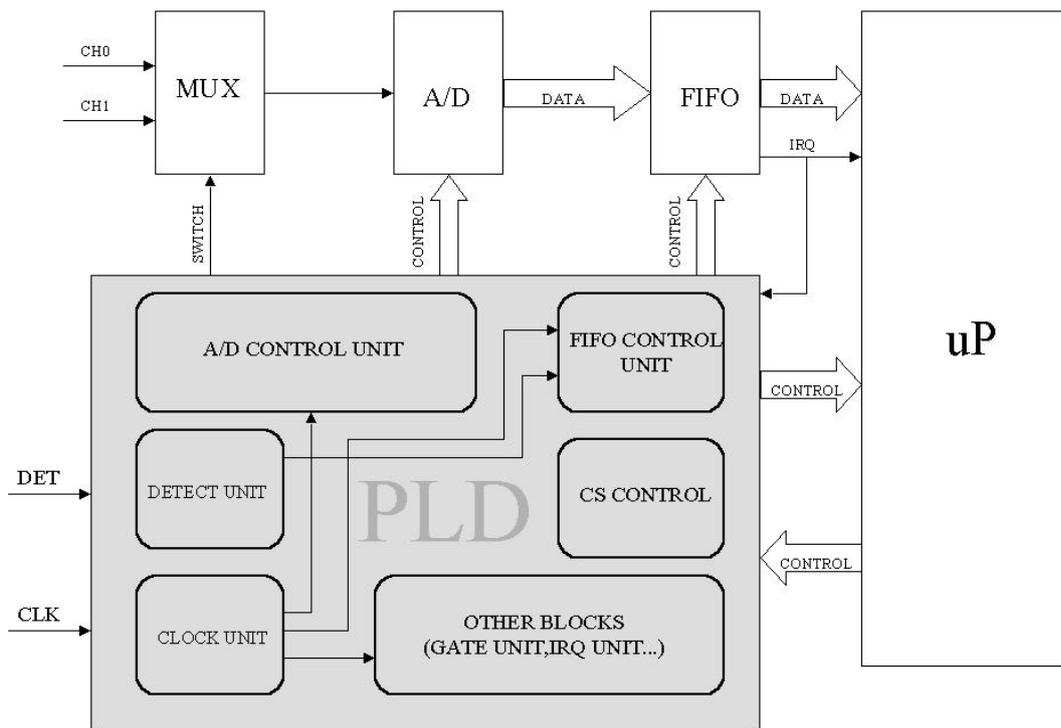


Fig.3. Block diagram of stimulator pulse recording circuit.

Development of implanted heart stimulators regarding the functionality enforced a few essential circuit changes of measurement interface. Among the most important is the possibility of ECG recording in case of four stimulator pulses. Moreover, to improve the recording quality of

form of pulses with strongly differentiated amplitudes, two measurement channels with separately programmed amplification have been applied (Fig. 4).

Each measurement channel consists of two ECG leads, so four channels undergone the signal conversion. Single analog-to-digital converter (with sampling frequency 400 kHz) and multiplexer switching the consecutive channels to converter were used. In relation to former version of measurement interface, the converter was changed from parallel to serial one. The capacity of FIFO memory has been enlarged four times. All these changes have substantially complicated the peripheral circuit regarding the logic.

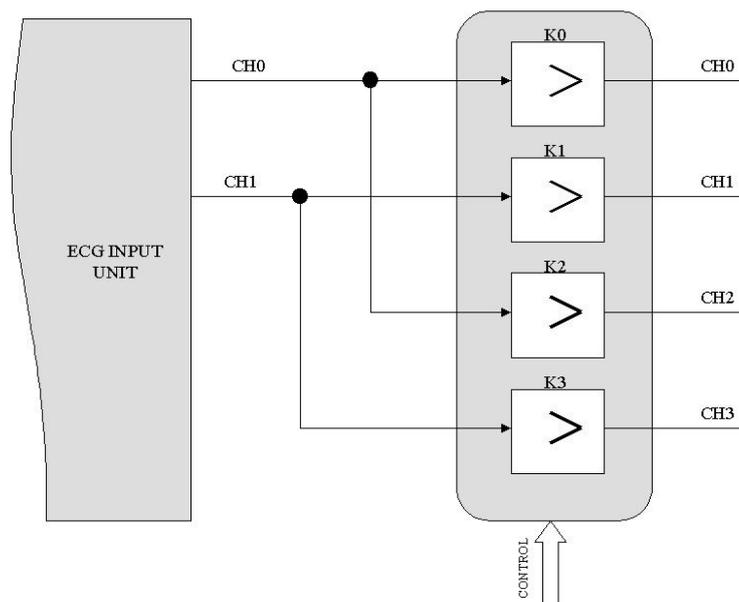


Fig.4. Measurement channels of stimulator pulse.

For further integration, the FIFO memory has been embedded in PLD circuit apart from standard logic, a few Serial Peripheral Interface (SPI) circuits used to communicate with converters and digital potentiometers and other modules. In addition, to enable the modification of logic structure in the devices already used by a client (e.g. via Internet) the configuration program has been enclosed in FLASH memory together with the processor program.

The interconnection configuration is done by the Passive Parallel (PP) method at the moment of processor initialization. The FLASH memory, which means the processor program and PLD structure configuration, can be reprogrammed from the level of IMPULS system application. To cope with the tasks assigned to peripheral circuit, the representative from ACEX 1K family of Altera Company – EP1K30 (with basic resources shown in table 2) has been applied.

Feature	Typical gates	Maximum system gates	Logic elements (LEs)	EABs	Total RAM bits	Maximum user I/O pins
EP1K30	30 000	119 000	1728	6	24 576	171

Tab.2. Features of EP1K30 circuit.

Block diagram of new measurement interface is shown in Fig. 5.

The basic modules designed in PLD structure are:

- module of double signal buffering,
- module of separation of signals activating particular circuit elements,
- module of pulses converter control together with selection of ECG lead,
- module of stimulator pulses detection,
- module of communication with main system processor,
- module of test signal generation.

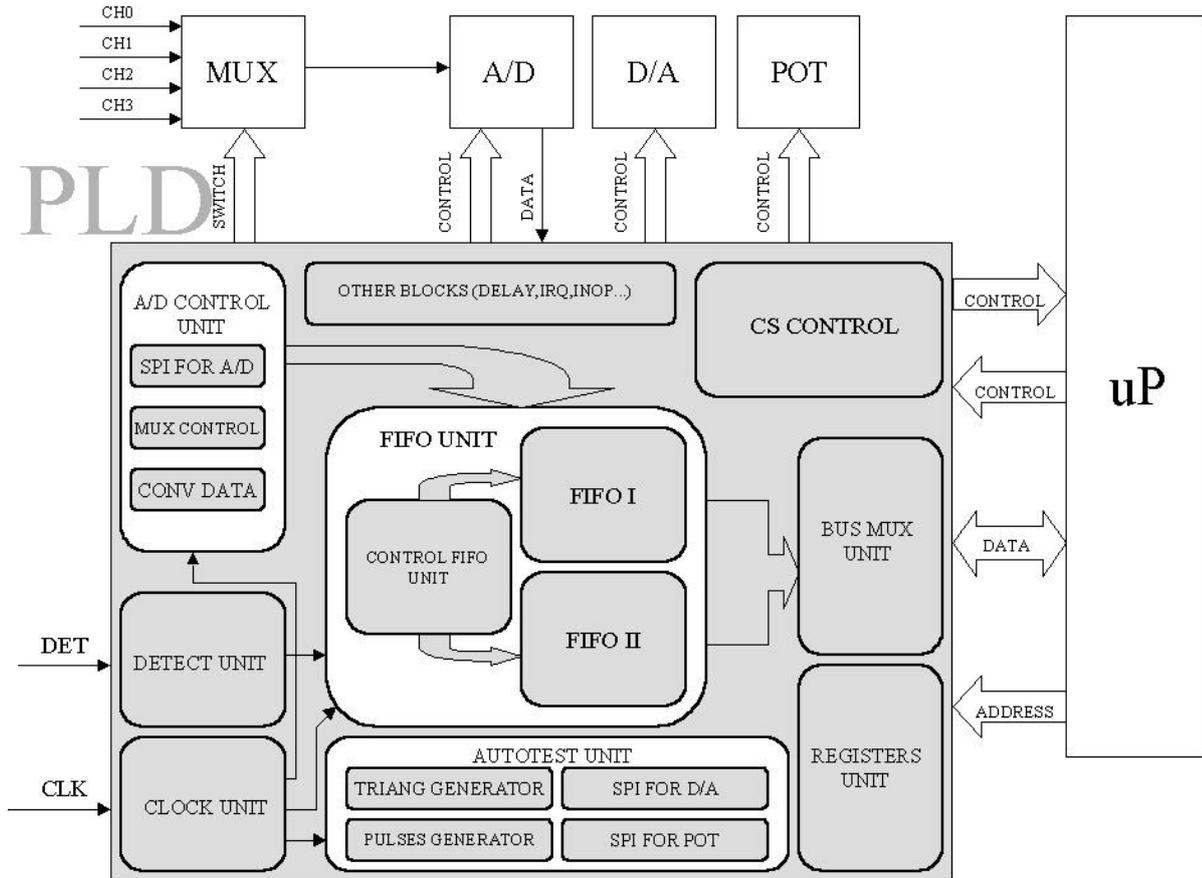


Fig.5. Block diagram of measurement interface.

Module of fast pulse converter control by means of SPI serial bus receives sampled values of ECG signal. Four signal channels are being scanned. At the moment of pulse detection (by detection module), the signals from all channel are recorded in actually free FIFO memory (in the block of double signal buffering). Because the latest stimulators are able to generate pulses in short time periods, two memory circuits working alternatively were used to enable the system to receive and convert this type of signal. In order to suppress the interference of analog signals with digital ones, there was applied the module of separation of signals controlling such elements as: converters, digital potentiometers etc. Bus signals of SPI interface are routed only to the actually controlled element.

The main processor communicates with programmable circuit by means of separated block of read/write registers as well as by means of independent control signals and hardware interrupt lines.

During the processing of received signals, the main processor is using almost whole computing capacity, therefore, it is not able simultaneously to generate, receive, process and send the autotest signal to the computer. Due to this reason, in the PLD circuit, there has been included the autonomic module of test signal generation that – initialized by main processor – takes over the realisation of this function. The module controls the digital-to-analog converter and digital potentiometer in order to establish proper amplitude. By means of a special plug inserted in site of patient's cable, the analog signal is returned to the measurement interface input and treated as ECG with artefacts of two pulses. Fig. 6 presents the test waveform.

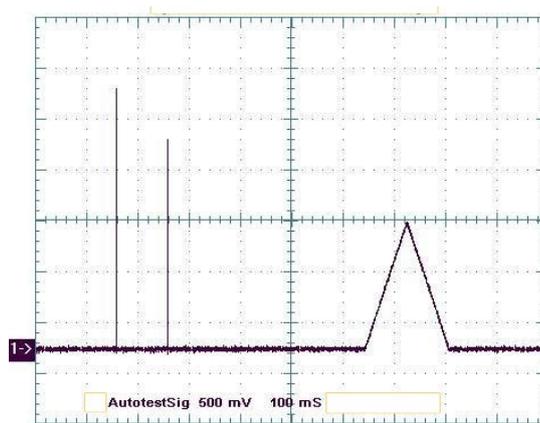


Fig.6. Test signal generated by PLD

Apart from the described blocks, the EP1K30 circuit structure processes various signals controlling the peripherals run (generates delays, elongates signals duration, performs basic logic functions). Taking into account the number of tasks realised beyond the processor, it is hard to imagine the use of conventional elements in this case.

4. FUTURE DEVELOPMENT

Fast changing of client's requirements and growing level of functional complexity of stimulators enforce the necessity of fast adaptation of interface construction to actual needs. The design-implementation cycle can be essentially shortened by further integration of maximum number of elements. One of possible concepts is to embed the device's digital part into one integrated circuit – System On a Programmable Chip (SOPC) [3]. Nowadays, these solutions are proposed by most of PLD producers and they can be divided into two groups: in the first group the implemented microprocessor is a physical element of integrated circuit structure, in the second one the processor is implemented in programmed way. In this approach, the processor components (central unit, counters, registers, UART, SPI, etc.) are created at the moment of PLD circuit programming when configuring interconnections.

In the first case, it is possible to achieve better processor efficiency but the designer is constricted by a given type of PLD circuit only. In the second case, the designer has wider choice of

elements because he can implement constructed processor to the larger group of PLD circuits and he is not connected with the sole type or family of circuits. Block diagram of exemplary SOPC is shown in Fig. 7.

Recently, the preliminary works are conducted to specify further design directions in outlined area. In present medical technology and market situation, the construction of system based on the second method of processor implementation into SOPC seems to be a better idea. This way of digital device design enables implementation of various programming methods (e.g. neural networks, parallel processing) into logic structures. Algorithms requiring large processor capacity can be hardware-implemented utilising parallel run of many modules of the SOPC circuit.

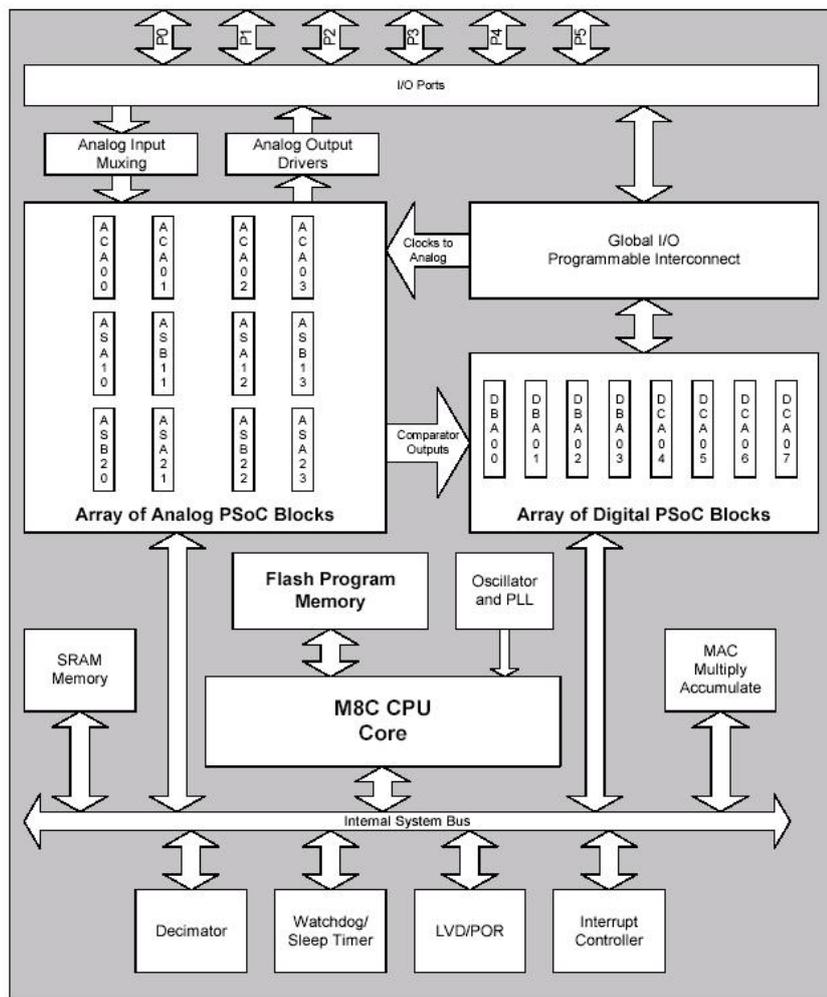


Fig.7. Block diagram of example SOPC [5]

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