

*Remote laboratory, distance learning,
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IDIPHASO E-LEARNING SYSTEM – ACCESS TO SOFTWARE TOOLS FOR DIGITAL DESIGN

In our paper we present the INDIPHASO [1] e-learning system for the design of digital systems implemented using FPGAs or CPLDs. The system allows users to access remotely, from a computer connected to the Internet, developing boards based on programmable logic circuits and microcontrollers in order to implement their designs. The paper describes the way the users can access the software tools in order to perform the steps in a predefined or a custom design flow. The three described methods provide different levels of accessibility and possibility of design flow configuration.

1. INTRODUCTION

We present an e-learning system denoted INDIPHASO [1] consisting of a set of web-based tools permitting remote configuration and test of hardware-software applications implemented using XESS prototyping boards (XSBs) [2]. The tools denoted as Remote XSTools (RXST) [3] provide a set of web-based interfaces to the XESS XSTools [4]. Using RXST users have access to the 4 XSBs, each one equipped with a XILINX programmable integrated circuit (FPGA or CPLD) and an 8031 microcontroller (μ C)[2]. They can configure remotely the programmable circuit and load an executable file for the microcontroller in order to implement different digital designs and test their operation.

RXST consists of a set of web-based interfaces for the XESS XSTools providing similar look and functionality. Mixed hardware-software designs can be experimented remotely by partitioning the application into modules that are either hardware implemented (FPGA/CPLD) or software implemented as a program loaded into the memory of the μ C.

Some versions of the design tools are available free from the programmable circuit vendors. The Xilinx company offers the WebPack [5] software for designing with CPLDs and also with Spartan and Virtex FPGAs. Students can install this software on their computer at home in order to design their applications to be implemented in the programmable circuits on the XSB. For some students this is not possible because they don't have a computer or because their computers lack the features requested by the software (high processor speed, large hard disk space, big RAM). In this case the e-learning system gives them the possibility to access the design software installed on the computers in the laboratory.

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In this paper we present the modality in which the e-learning system gives students the possibility to synthesize and implement their design specified using VHDL or Verilog hardware description languages.

2. INDIPHASO E-LEARNING SYSTEM

The INDIPHASO e-learning system is organized around the equipment used for normal student laboratory work platforms consisting of:

- personal computers connected to the Internet;
- XESS prototyping boards - four types [1]: XS40-005XL, XS40-010E, XS95-108 and XSA-50;
- microcontroller-based development boards;
- digital multimeters, oscilloscopes, signal generators etc.

Table 1 summarize the features of the four prototyping boards. As we can see XS40-005XL, XS40-010E, XS95-108 boards have a programmable circuit and a microcontroller while the XSA-50 board has two programmable circuits.

Features	XS40-005XL	XS40-10E	XS95-108	XSA-50
FPGA	XC 4005XL	XC 4010E	No	XC2S50
CPLD	No	No	XC 95108	XC 9572XL
Microcontroller	8031	8031	8031	No
RAM	32Kb	128Kb	128kB	16MB
Flash	No	No	No	256kB
Parallel port	Yes	Yes	Yes	Yes
VGA port	Yes	Yes	Yes	Yes
PS/2 port	Yes	Yes	Yes	Yes
Programmable oscillator	Yes	Yes	Yes	Yes
7-segment LED	Yes	Yes	Yes	Yes
Push-button	No	No	No	Yes
Serial EEPROM socket	Yes	Yes	No	No

The laboratory works require the use of different software tools in order to:

- design the hardware part to be implemented in the programmable circuits (FPGA or CPLD);
- write and debug programs for the microcontrollers on the XSBoards or on the microcontroller based development boards (programs can be written in C or assembler language);
- configure of the onboard programmable circuit(s);
- load microcontroller program into memory;
- test the design by sending test vectors to the board.

In the laboratory we use the following software tools:

- Xilinx Foundation version 1.5i which can be used for hardware design and for generating the configuration files for FPGAs (XC4000 family) and CPLDs;
- Xilinx Webpack software tools which can be used for programming the CPLDs and Spartan-II FPGAs.

- Franklin Software is used for writing and debugging the programs for the 8031 microcontroller. The program can be written in assembler language but a C compiler is also available.
- XESS Tools is the software provided by the manufacturer of the prototyping boards a) xsload - the tool used for downloading designs into the XSBoard. It is used for downloading both the hardware and software design. It can also be used to read back the design stored on the board; b) xstest - used for testing the correct operation of the board; c) xssetclk - used to set the on-board programmable clock; d) xsport - used for applying test signals to XSBoards using the PC parallel port.
- The web server Apache v.2.0 is installed on the server in order to serve the web-based tools.
The architecture of the e-learning system is depicted in Fig.1 and its operation is described in greater detail in [1].

3. ACCESS TO SOFTWARE TOOLS

The Xilinx company offers the WebPack software for designing with CPLDs and also with Spartan and Virtex FPGAs. Students that do not have the designing software or can not use it because of hardware/software limitations of their computers (slow processor, small hard disks, low RAM memory) can access the free or licensed copies installed on the computers in the laboratory.

In order to give access to the design software tools, necessary to implement applications using Xilinx FPGAs and CPLDs found on the XSB, we have tested three solutions:

- using Xilinx XFLOW program [xflow]. XFLOW program allows user to automate implementation and automation flows using Xilinx tools;
- using MAKE utility and defining a user flow that runs the Xilinx design tools specified in a Make file;
- using VNC (Virtual Network Computing) [8] server on the computer where are installed the design tools. Using the VNC viewer (the VNC corresponding client) the user gets access to the Xilinx Synthesis Technology design system or to available individual tools for synthesis, implementation and configuration.

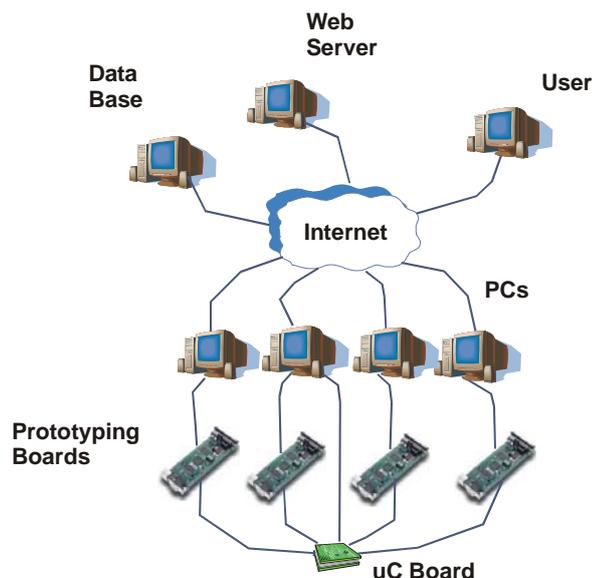


Fig. 1. System architecture.

Remote access to the software tools is allowed only to the registered users (students) of the Indiphaso e-learning system.

3.1. USING XFLOW

XFLOW program was developed by Xilinx in order to help users to automate implementation and simulation of digital design using the Xilinx tools. Using XFLOW, which is a command line program, design can be performed without working with the graphical interface provided by the integrated environment included in Xilind ISE family design packages.

Running XFLOW implies the specification of the command line parameters following the syntax given in the documentation. These parameters are:

- part name: the part name of the circuit in which the design will be implemented,
- flow type: specifies the type of design flow to be executed,
- option file: include the option for the programs run in the flow. The programs perform design tasks such as synthesis, mapping, place and route, configuration generation, but can also execute any other program specified by the user.
- xflow option: options for the XFLOW program,
- design name: the name of the top level design name.

More details about the parameters can be found in [5]. XFLOW allows different flow types for synthesis, implementation, and simulation of the design as well as for the generation of the configuration file. Three different flow files are associated with flow types, containing specific commands and parameters for designing with FPGAs, CPLDs or for simulation.

In our system we provide a set of option files which the user can utilize in his design. In the case of synthesis, there are available option files that can be used to do design optimisation minimising either speed or area. Separate option files are available for the case the design is described using VHDL or Verilog.

Advanced users can modify the option files in order to implement other optimization strategies.

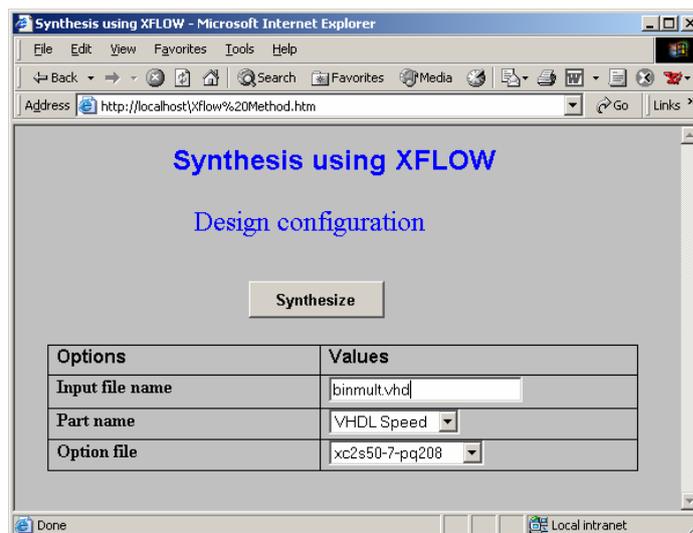


Fig. 2. Synthesis using XFLOW web form.

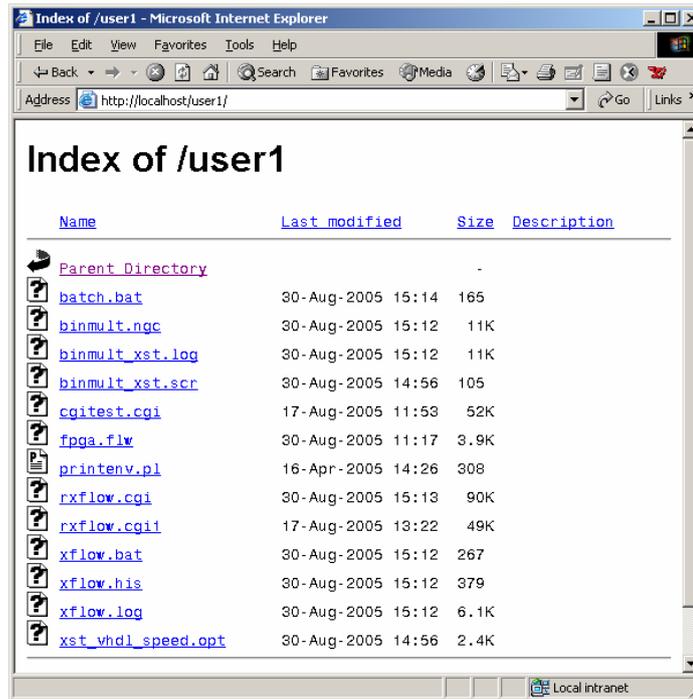


Fig. 3. Access to files generated by XFLOW.

Fig. 2 depicts the web form where users must provide the parameters for the synthesis using XFLOW. Once the parameters are set, the XFLOW command is executed by a cgi script. When the XFLOW commands completes, the CGI script displays in user's browser the working folder where were created the files generated by the XFLOW program (Fig.3). XFLOW user guide [5] describes each of the generated files. Of great importance is the LOG file which contains the messages generated by the program during execution. Reading this file the user can see if the synthesis was done without error or in the opposite case, what the error are.

A web form similar with the one depicted in Fig.2 is provided for the implementation and generation of the configuration file. For the moment simulation option of XFLOW is not supported by the e-learning system.

3.2. USING MAKE

The second method to remotely access the design software tools is using the well-known Unix utility, MAKE. The method was inspired from [6] and was adapted to work with Xilinx WebPack tools and to be used remotely from a computer connected to Internet.

The method implies the creation of a Makefile script either manually or using a web form. The make file will contain the command lines for running the design tools (synthesis, translation, mapping, place and route, generation of configuration file) and the option for each program which can implement different design strategies. In addition other user commands can be added and configured (creating and removing temporary files or folders, setting environment parameters, generating reports and issuing execution or error messages).

Our e-learning system uses Xst program [7] for the synthesis of HDL files written in VHDL and Verilog. Running Xst in command line implies the specification of a large number of options. Instead of providing manually these options, we can specify a script file where every option can be set to the appropriate value. Therefore, we have created a CGI script associated to the configuration web form that will create a Makefile. When running the MAKE utility on the Makefile, a .scr script file will be created containing the options for the Xst program. The Makefile file will contain the

command line for the Xst and the command lines and options for the other software tools in the package (NGDBUILD, MAP, PAR, TRACE, BITGEN). For each of the parameters not specified in the web form, the CGI script assumes the default values.

The web form allows the user to provide its custom Makefile. This feature is useful in the cases when the user options differ from the default values. An easy way to work with the make utility is to use the web form to specify the option for each parameter and then saving a copy of the generated Makefile. If minor changes are to be made on the set of options, the user can edit manually the Makefile.

Global Options	Values
Input file name	binmult.vhd
Input file name format	VHDL
Output file name	
Case	Lower
Hierarchy Separator	_
Optimization Goal	Speed
Optimization Effort	1
Target Technology	xc2s50-7-pq208
Generate RTL Schematic	No
Ignore User Constraints	No
Synthesis Constraints File	

Fig. 4. Synthesis using MAKE web form.

3.3. USING VNC

VNC [8] is a remote display system that allows a user to view and interact with the desktop of a remote machine running, anywhere on the Internet. Different extensions of VNC have been developed and numerous new features have been added to the software.

In our e-learning system, VNC can be used to access the Xilinx design software tools in this way taking benefits of the graphical user interface of the designing modules.

For the moment we have used RealVNC which, in the Windows version running on a Windows 98 machine, allows only one active desktop therefore, only one user can access the designing software tools at a time.

Figure 5 shows accessing Xilinx WebPack designing tools on a server in e-learning system laboratory running VNC server (VNCserver) from a computer connected to Internet running the VNC client (VNCviewer). In this case the user has full access to GUI and can work with the software tool in the usual graphical mode.

4. CONCLUSIONS

In this paper we have described the INDIPHASO e-learning system developed to allow the development of digital applications implemented on remote prototyping boards based on programmable logic circuits. We have presented three methods that the users of the e-learning system can use to access over the Internet the Xilinx designing software tools running on the server in the e-learning system laboratory.

The current version of the e-learning system gives access only to some of the designing software tools features therefore, further work will seek to extend system capability and improve system operation.

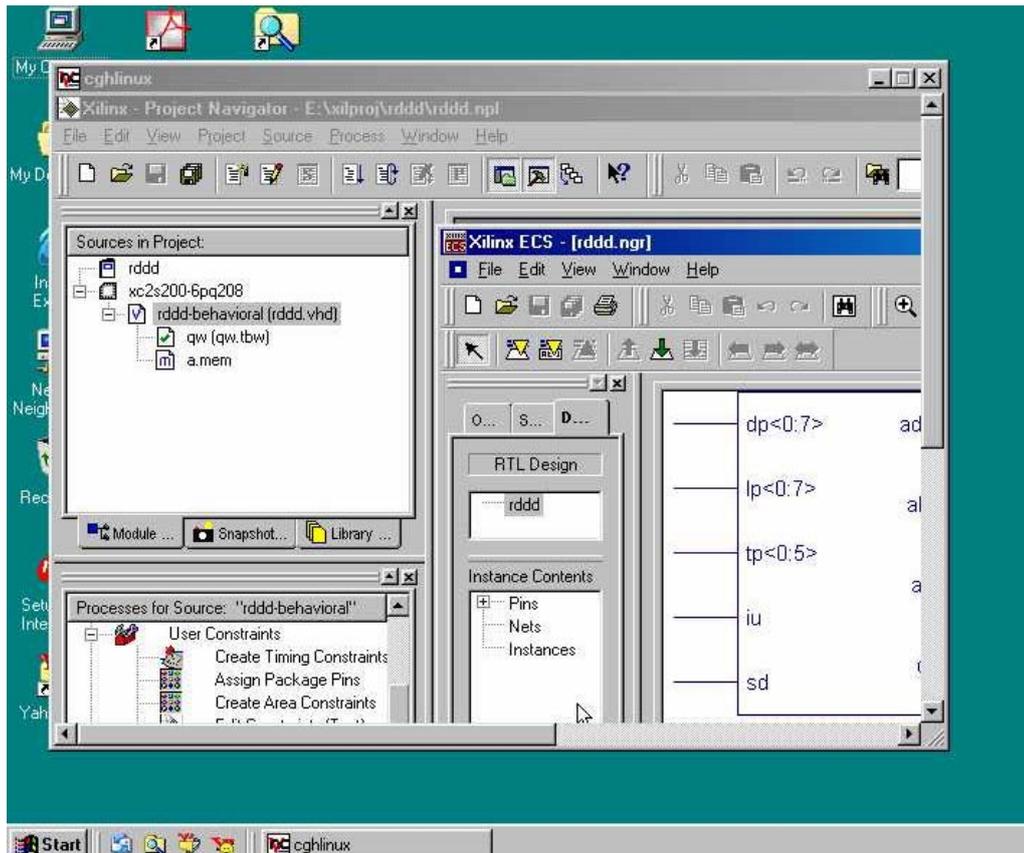


Fig. 5. Running Xilinx WebPack software remotely using VNC.

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